

Fig. 1

FIG. 2 is a block diagram of a system 120, in accordance with an embodiment of the present invention. The system 120 includes a processor 220, memory 230, storage 240, a spy 210, and a communication port 260. The processor 220, memory 230, and storage 240 are connected to an I/O bus 250. The spy 210 and the communication port 260 are also connected to the I/O bus 250.

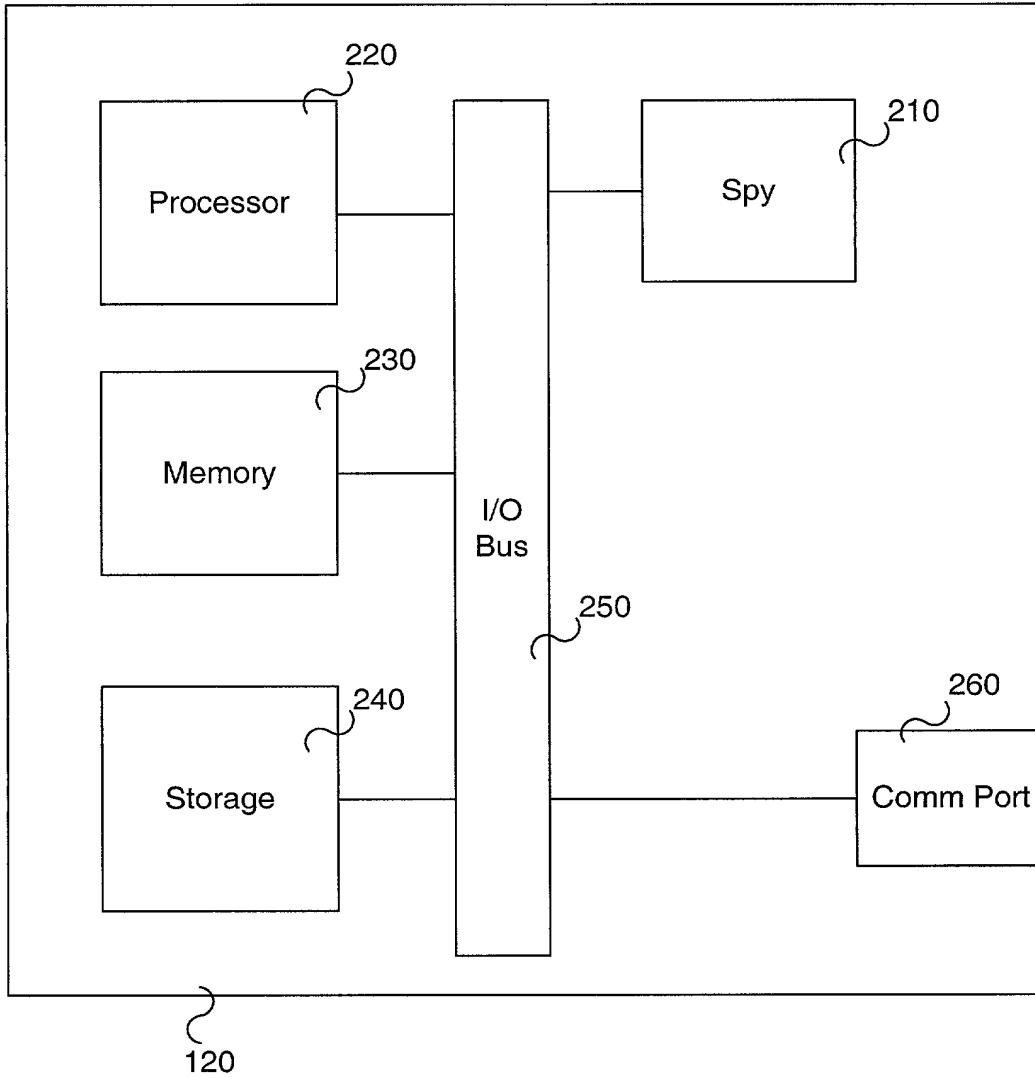


Fig. 2

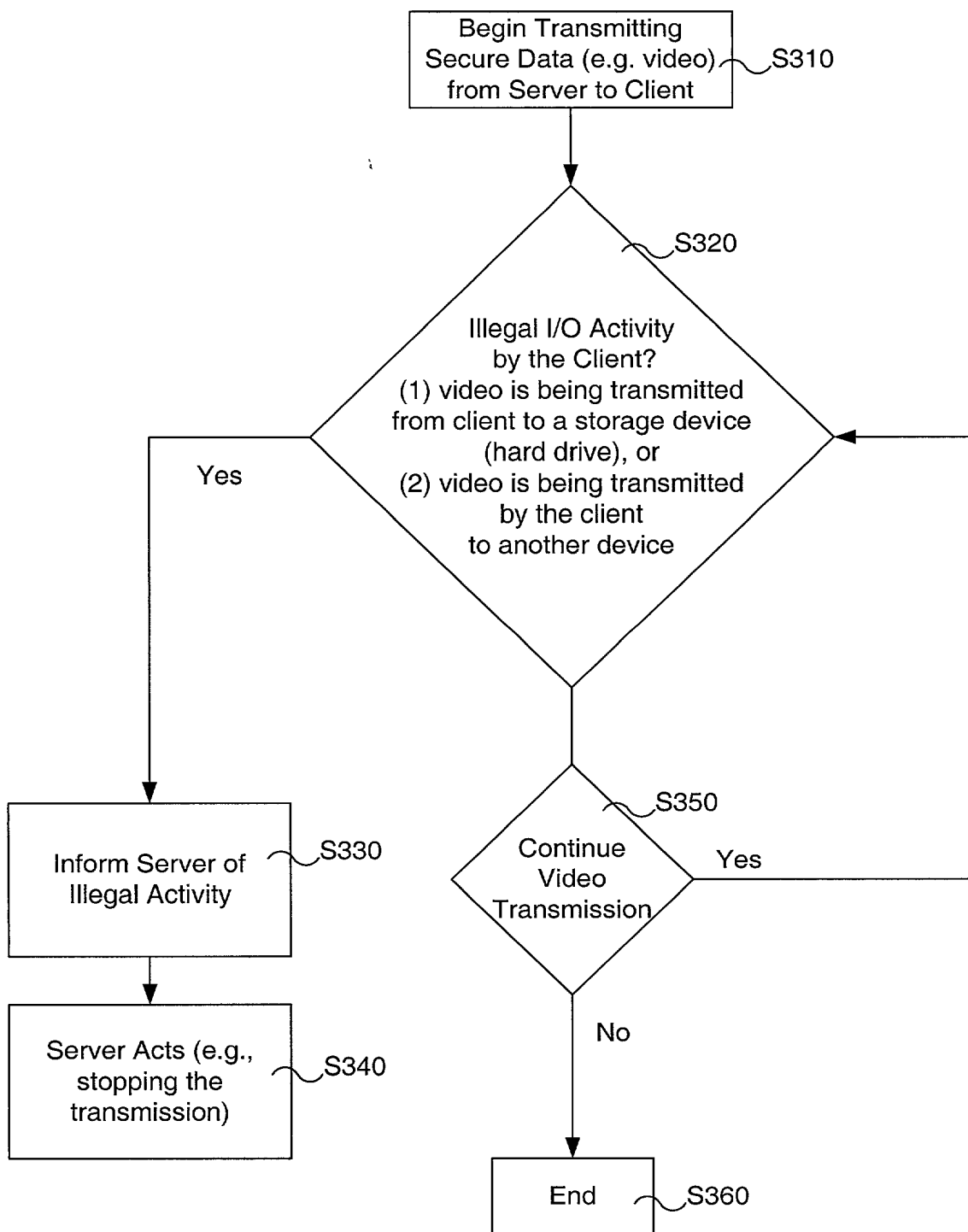


Fig. 3

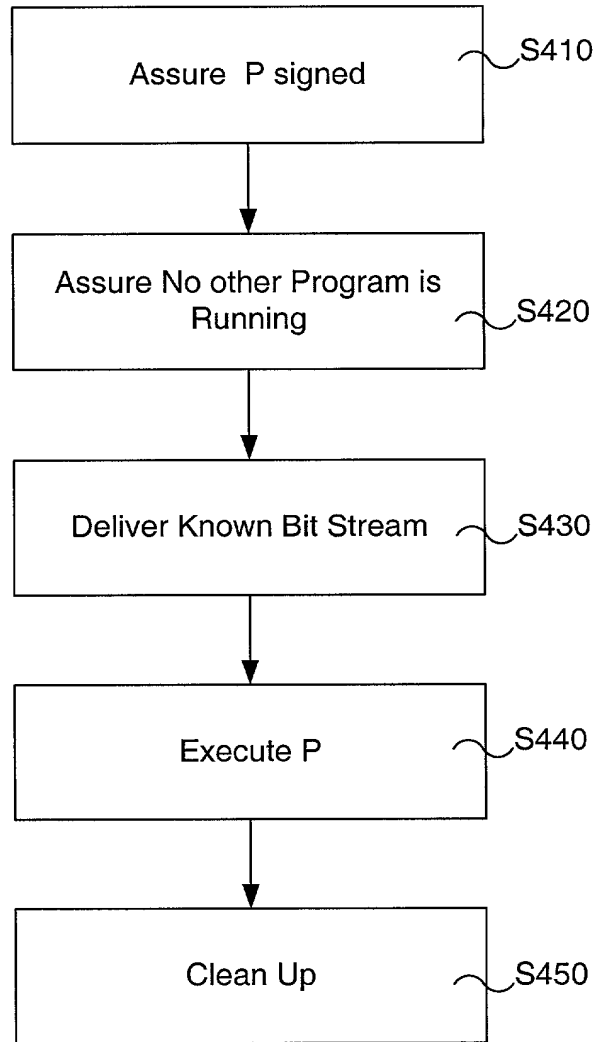


Fig. 4

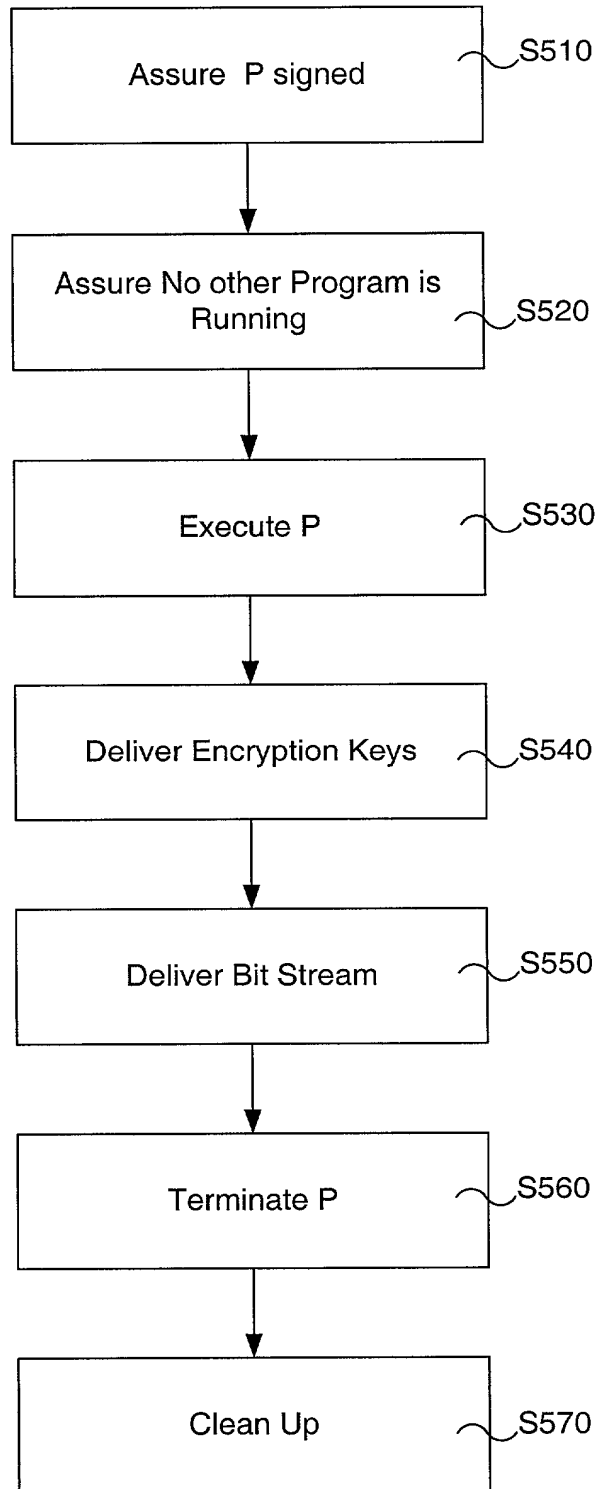


Fig. 5

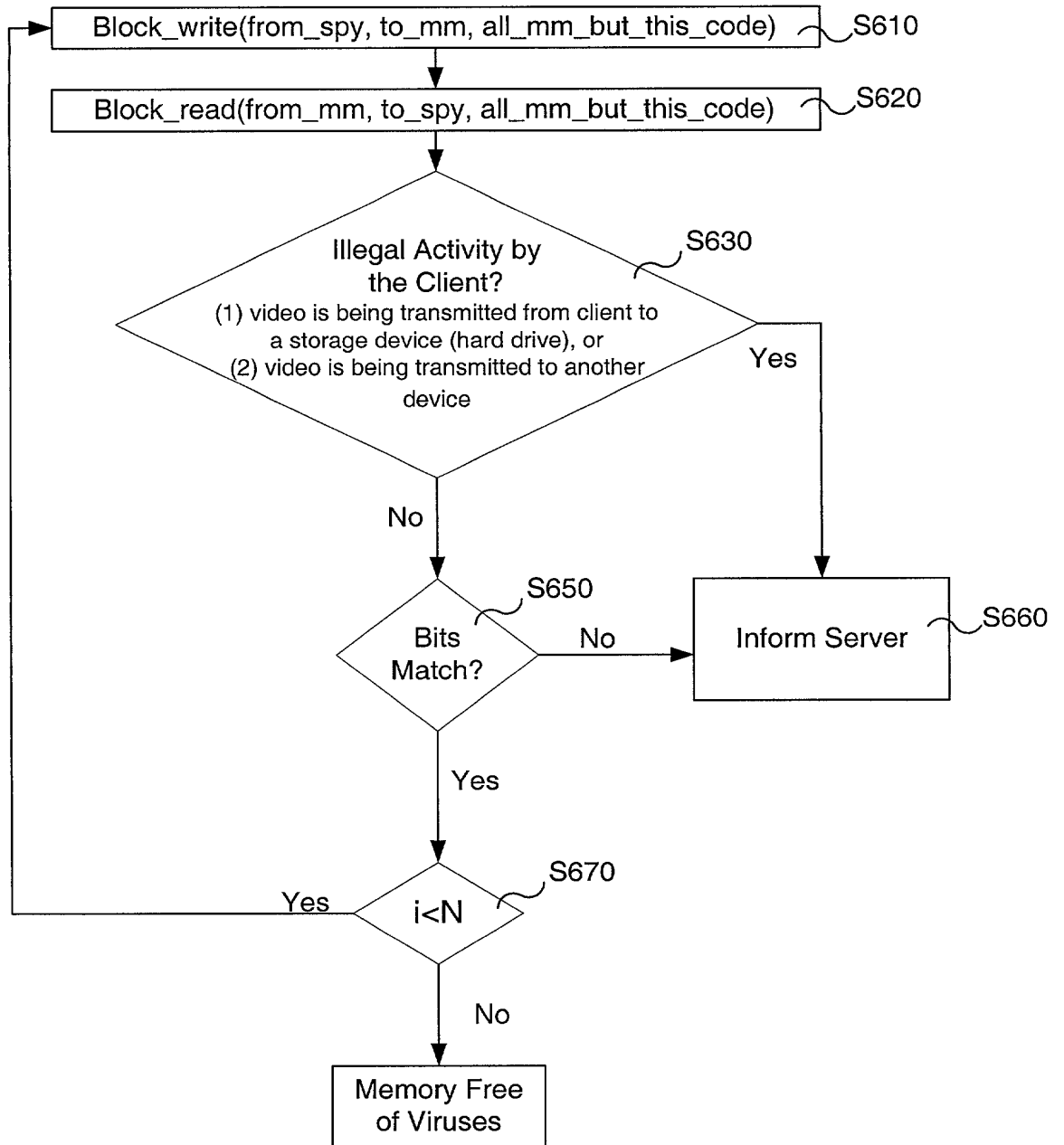


Fig. 6